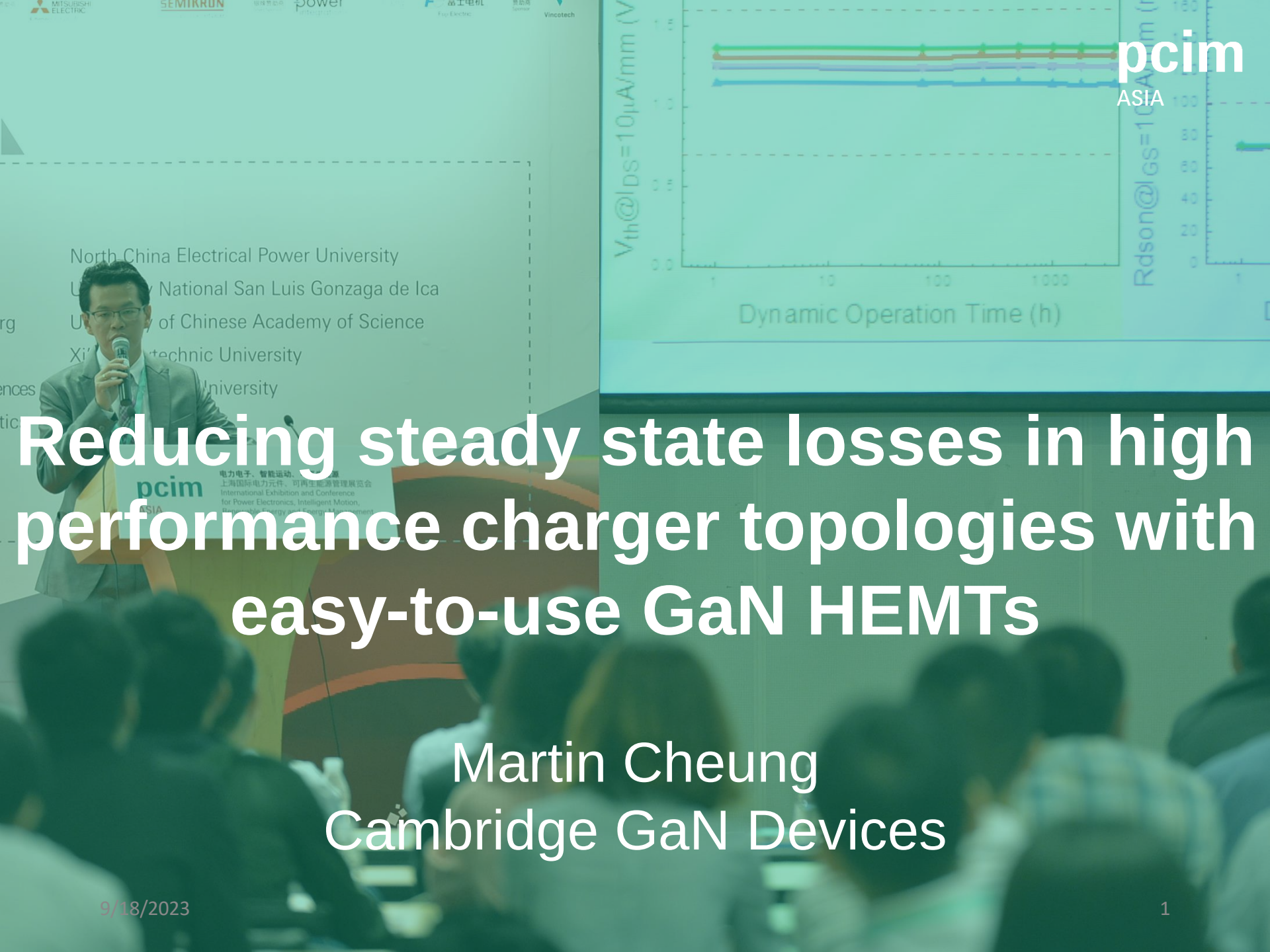



# Reducing steady state losses in high performance charger topologies with easy-to-use GaN HEMTs

Martin Cheung
Cambridge GaN Devices

# OUTLINE

- Chargers design trends
- Topologies review for chargers
- Easy-to-use GaN HEMTs charger design
- Measurement results

# Chargers design trends

# CHARGER DESIGN TRENDS

Environmental sustainability:

- Standardize dc power connector, USB Type-C
- Reduce no load input power and increase charger efficiency at 10 % loading to 100 % loading

Users' requests:

- Charger designs for universal ac input voltage and variable output dc voltage
- Smaller form factors and shorter the charging times

Therefore, charger design trends

- High efficiency (>93 % @ 100 Vac full load) with low no load power consumption
- Output power: >65 W
- Power density increase:
  - 65 W charger around 1.2 W/cm$^3$
  - 75 W to 240 W charger around 1 W/cm$^3$ (including PFC stage)

# SINGLE VOLTAGE EPS AC-DC

Efficiency in active mode – standard/basic voltage output (≥ 6 V)

| Output Power | DoE Level VI 2016 | | DoE* (Feb 2023) | CoC Tier 2 2016 | ErP 2020 | |
|---|---|---|---|---|---|---|
| | Efficiency | PF | Efficiency | Efficiency | Efficiency | PF |
| 0.3 W-1 W | ≥ 0.517 $P_{no}$ + 0.16 | | ≥ 0.517 $P_{no}$ + 0.091 | ≥ 0.5 $P_{no}$ + 0.169 | ≥ 0.5 $P_{no}$ + 0.16 | |
| 1 W – 49 W | ≥ 0.071 ln($P_{no}$) – 0.0014 $P_{no}$ + 0.67 | | ≥ 0.0834 ln($P_{no}$) – 0.0011 $P_{no}$ + 0.643 | ≥ 0.071 ln($P_{no}$) – 0.00115 $P_{no}$ + 0.67 | ≥ 0.071 ln($P_{no}$) – 0.0014 $P_{no}$ + 0.67 | |
| 49 W – 250 W | ≥ 0.88 | ≥ 0.9 at 115 $V_{ac}$ /60 Hz for $P_{in}$ ≥ 100 W | ≥ 0.902 | ≥ 0.89 | ≥ 0.88 | EN-61000-3-2 Class D |
| >250 W | ≥ 0.875 | | ≥ 0.902 | N/A | N/A | |

No load power consumption – low voltage output and standard/basic voltage output

| Output Power | DoE Level VI 2016 | DoE* (Feb 2023) | CoC Tier 2 2016 | ErP 2020 |
|---|---|---|---|---|
| 0.3 W-49 W | ≤ 100 mW | ≤ 75 mW | ≤ 75 mW | ≤ 100 mW |
| 49 W – 250 W | ≤ 210 mW | ≤ 75 mW | ≤ 150 mW | ≤ 210 mW |
| >250 W | ≤ 500 mW | ≤ 200 mW | N/A | N/A |

$P_{no}$: rated output power

*https://www.govinfo.gov/content/pkg/FR-2023-02-02/pdf/2023-01282.pdf

# MULTIPLE VOLTAGE EPS AC-DC

Efficiency in active mode

| Output Power | DoE Level VI 2016 | | DoE* (Feb 2023) | ErP 2020 | |
|---|---|---|---|---|---|
| | Efficiency | PF | Efficiency | Efficiency | PF |
| 0.3 W- 1 W | ≥ 0.497 $P_{no}$ + 0.067 | | ≥ 0.497 $P_{no}$ + 0.067 | ≥ 0.497 $P_{no}$ + 0.067 | |
| 1 W – 49 W | ≥ 0.075 ln($P_{no}$) + 0.561 | | ≥ 0.0782 ln($P_{no}$)- 0.0013 $P_{no}$+ 0.643 | ≥ 0.075 ln($P_{no}$) + 0.561 | |
| 49 W – 250 W | ≥ 0.86 | ≥ 0.9 at 115 Vac /60 Hz for Pin ≥ 100 W | ≥ 0.885 | ≥ 0.86 | EN-61000-3-2 Class D |
| >250 W | ≥ 0.86 | | ≥ 0.885 | N/A | |

No load power consumption – low voltage output and standard/basic voltage output

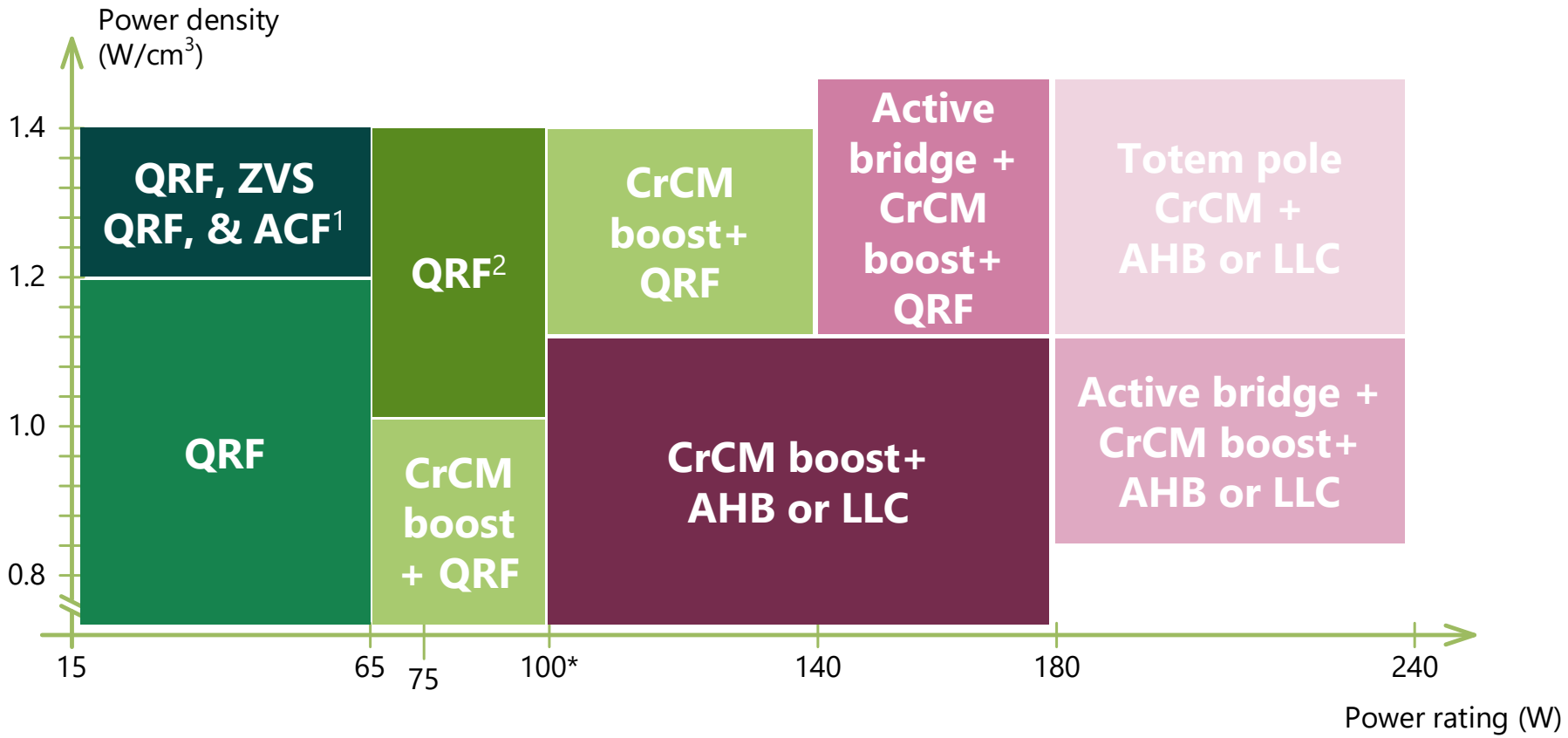
| Output Power | DoE Level VI 2016 | DoE* (Feb 2023) | ErP 2020 |
|---|---|---|---|
| 0.3 W-49 W | ≤ 300 mW | ≤ 75 mW | ≤ 300 mW |
| 49 W – 250 W | ≤ 300 mW | ≤ 125 mW | ≤ 300 mW |
| >250 W | ≤ 300 mW | ≤ 125 mW | N/A |

$P_{no}$: rated output power

*https://www.govinfo.gov/content/pkg/FR-2023-02-02/pdf/2023-01282.pdf

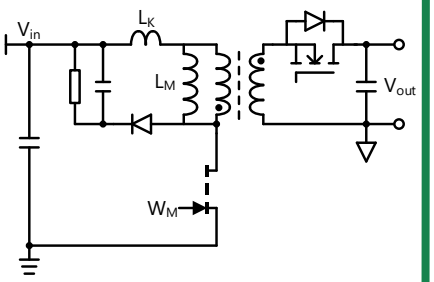
# Topologies review for chargers

# OUTPUT POWER VS TOPOLOGIES




Remark: *input power rating
Remark: 1. ZVS QR and active-clamp flyback are usually designed for 65 W chargers. QR flyback is used when the output power is below 65 W
Remark: 2. Power factor is not required in DoE Level VI 2016 when input power below 100 W

# FEATURES AND CHALLENGES FOR DC DC TOPOLOGIES



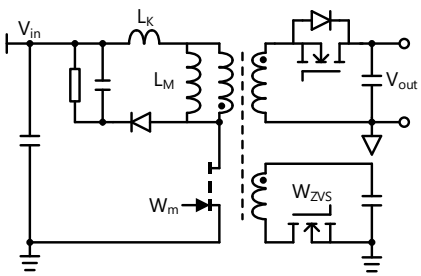

## QR flyback

Features:

1. Low cost
2. Minimize component count
3. Easy control
4. Well–known EMI
5. Low no load input power

Challenges:

1. High switching losses
2. High voltage stress at main switch
3. No leakage energy recycle



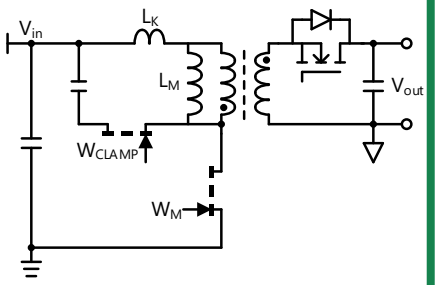

## ZVS QR flyback

Features:

1. ZVS at HV switch
2. Similar control as QR flyback
3. Well-known EMI

Challenges:

1. High voltage stress at main switch
2. No leakage energy recycle
3. High component count
4. High no load input power



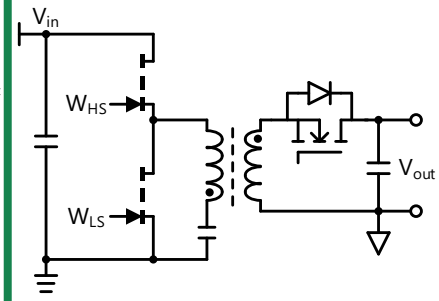

## Active clamp flyback

Features:

1. ZVS at HV switches
2. Low voltage stress in switches
3. Leakage energy recycle

Challenges:

1. Complex control
2. High component count
3. High no load input power




## Asymmetrical half-bridge

Features:

1. ZVS at HV switches
2. Low voltage stress and peak current stress in switches
3. Leakage energy recycle

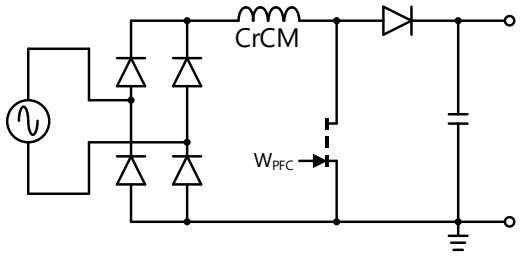
Challenges:

1. Complex control
2. High component count
3. High no load input power

# COMPARISON OF EACH DC DC FOR CHARGER DESIGNS

| Parameter | QR flyback | ZVS QR flyback | Active-clamp flyback (Complementary) | Asymmetrical half-bridge |
|---|---|---|---|---|
| Active component | • HV SW<br>• Low side driver | • HV SW<br>• LV SW<br>• 2 low side drivers | • 2 HV SWs<br>• Level shift driver<br>• Low side driver | • 2 HV SWs<br>• Level shift driver<br>• Low side driver |
| Passive component | • Transformer with additional winding for valley detection<br>• RCD Snubber | • Transformer with additional winding for ZVS<br>• Resonant capacitor<br>• RCD Snubber | • Transformer<br>• Clamping capacitor | • Transformer<br>• Resonant capacitor |
| Control complexity | • Simple | • Moderate | • Complex | • Complex |
| Leakage inductor energy | • Lost | • Lost | • Recuperated | • No leakage energy losses |
| ZVS of main SW | • Partially | • Almost | • Full | • Full |
| Full load efficiency | • Moderate | • Good | • Best | • Best |
| No load power (burst mode) | • Best | • Good | • Moderate | • Moderate |

# FEATURES AND CHALLENGES FOR PFC TOPOLOGIES



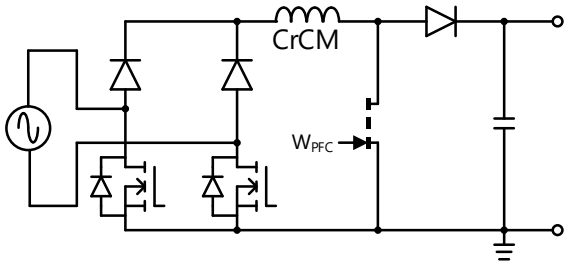

**CrCM boost**

Features:

1. Low cost
2. Minimize component count
3. Simple control
4. Well–known EMI

Challenges:

1. High rectifier bridge losses
2. High peak switch current
3. Limited output power



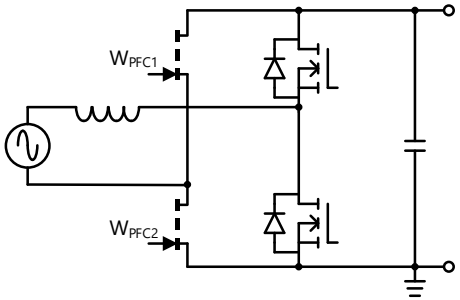

**Active bridge + CrCM boost**

Features:

1. Reduce bridge rectifier losses
2. Well-known EMI

Challenges:

1. High component count
2. High peak switches current
3. Cost




**CrCM/CCM totem pole boost**

Features:

1. No VF losses
2. High output power

Challenges:

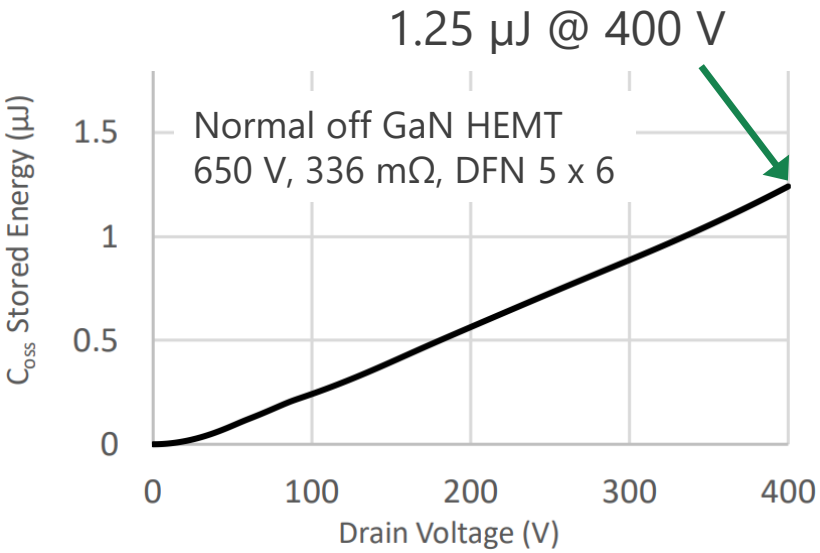
1. Floating driver
2. Complex control
3. EMI
4. Cost

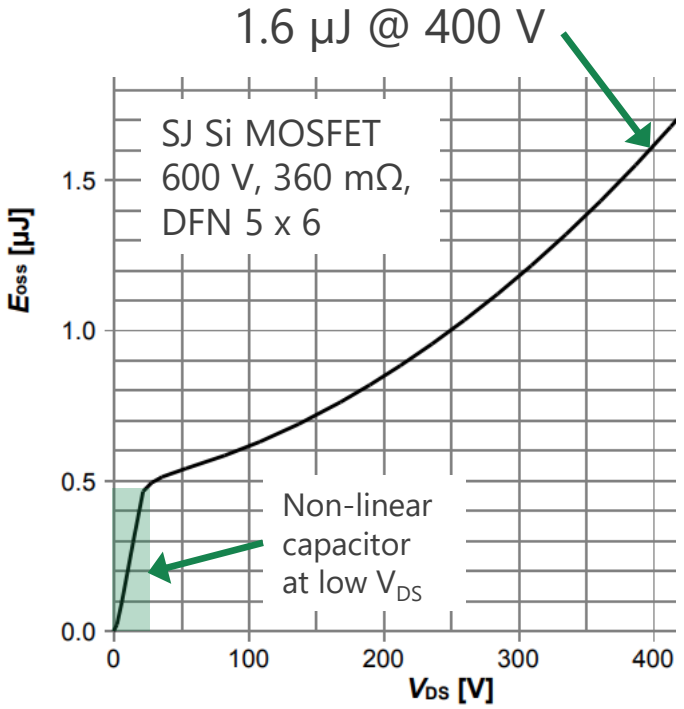
# Easy-to-use GaN HEMTs

# GAN HEMT VS SJ SILICON MOS

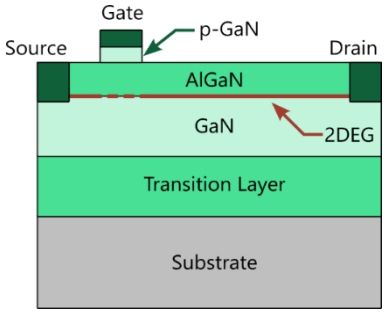
A small output capacitor, $C_{oss}$, with linear characteristic switching devices can provide

- low switching losses in hard switching
- easy to achieve zero voltage switching
- fast switching frequency



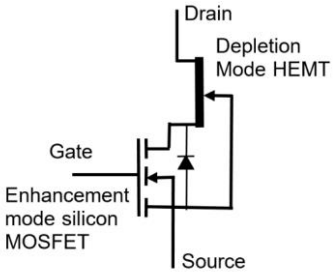
# EXISTING GAN HEMT SOLUTIONS




## DISCRETE

Features:
1. Normally off operation
2. Two types gate contacts Ohmic or Schottky

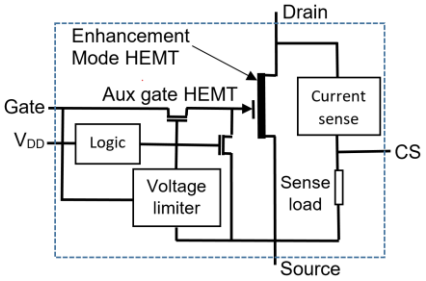
Challenges:
1. Low threshold voltage Vth~1.5 V
2. Low Vgs ~7 V
3. Negative driving voltages for turn-off




## CASCODE

Features:
1. Easy to use drive provided by the silicon MOS gate
2. Low on-state forward drop in the reverse conduction mode

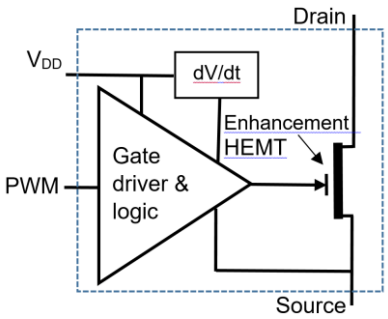
Challenges:
1. Reverse recovery losses at LV MOS
2. Slew rate control
3. High Qg




## Monolithic integration

Features:
1. Driving interface attached to the HEMT gate
2. Extended gate voltage up to 20 V
3. Miller clamp for turn-off

Challenges
1. Extra chip area for the interface
2. Required driver IC



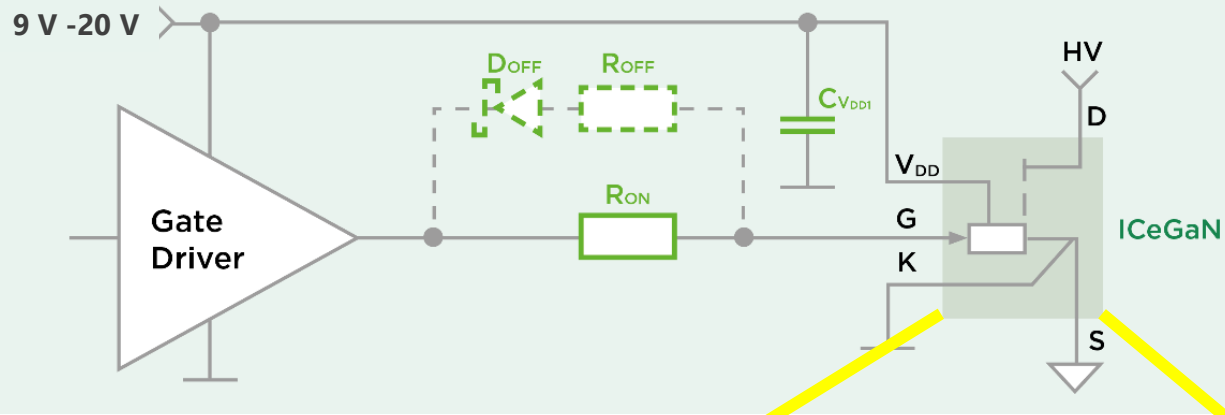

## Monolithic integration with driver

Features:
1. Robustness operation
2. Compact solution

Challenges:
1. Extra GaN chip area for the driver
2. Low driving current due to only n-channel LV GaN transistors is available (no p-channel).

# EASY-TO-USE GAN HEMTS

## Drive GaN like a MOSFET interface

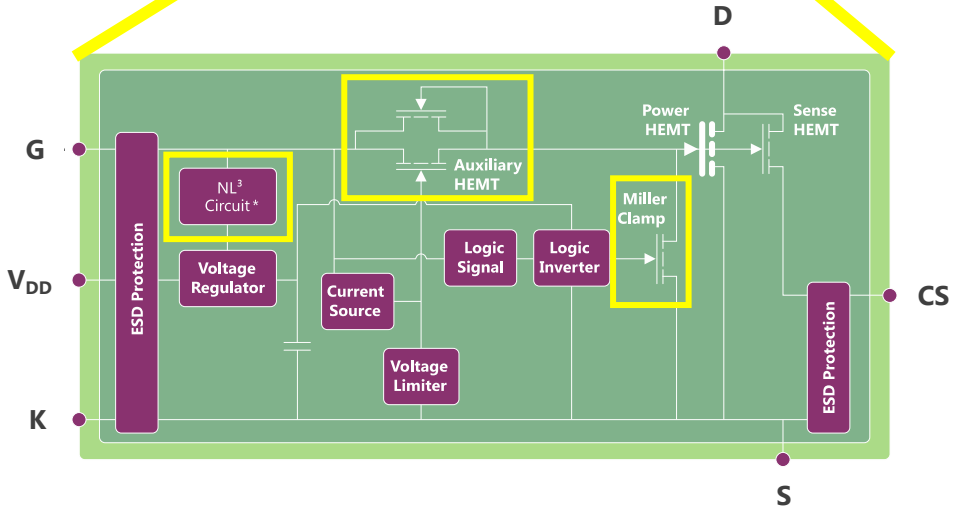



## NL³ Circuit:

Improve no-load conditions, burst mode, and light load efficiency

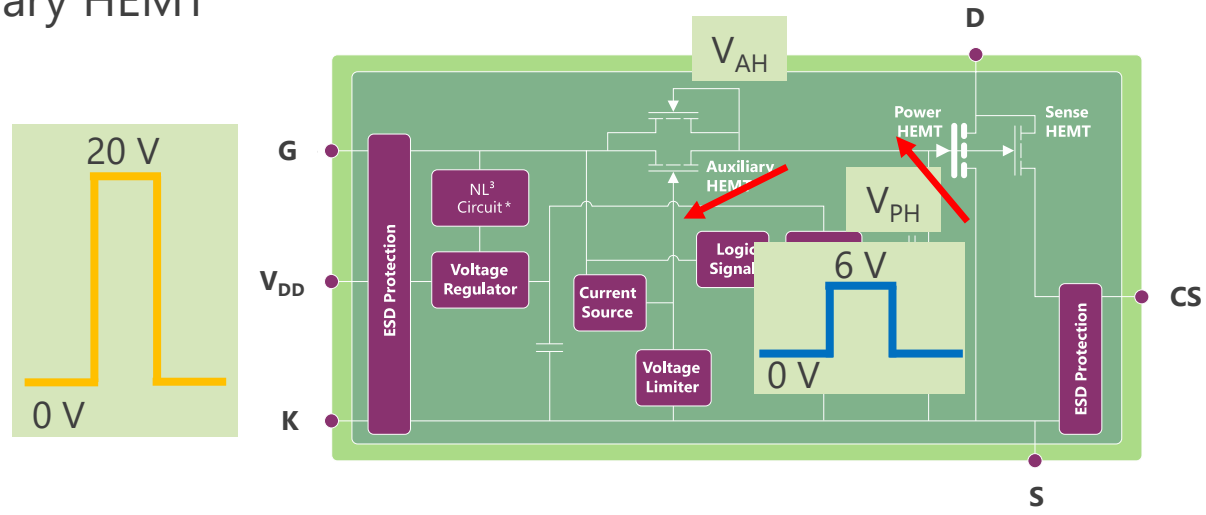
| | | | |
|---|---|---|---|
| $I_{VDD}$ | $V_{GS}$ = 12 V, $V_{DS}$= 0 V | 0.8 | mA |
| $I_{VDD}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 12 V, $V_{DS}$= 0 V | 0.4 | mA |
| $I_{VDD}$ | $V_{GS}$ = 0 V, $V_{DS}$= 0 V | 70 | µA |
| $I_{VDD}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 0 V, $V_{DS}$= 0 V | 35 | µA |

From datasheet CGD65B240SH2

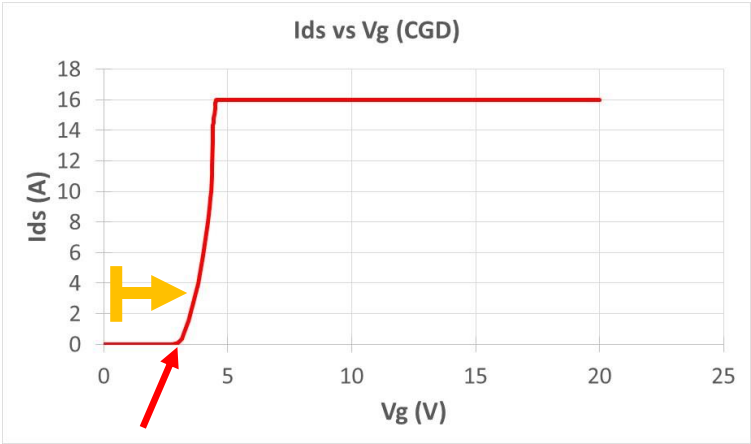


# EASY-TO-USE GAN HEMTS

## Auxiliary HEMT

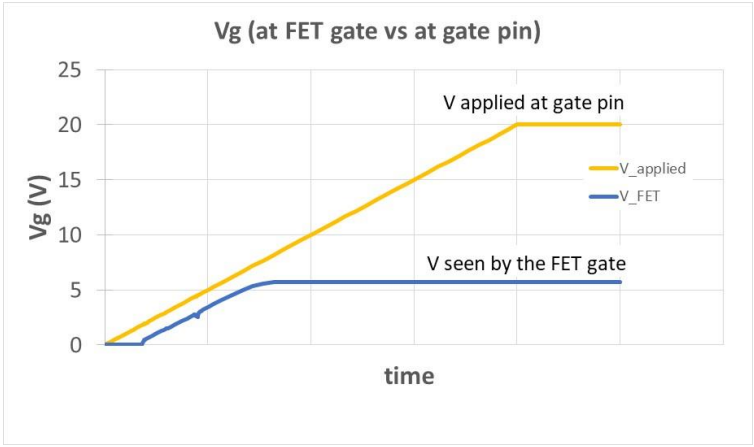



## Increase the threshold voltage




$V_{AH}+V_{PH}$

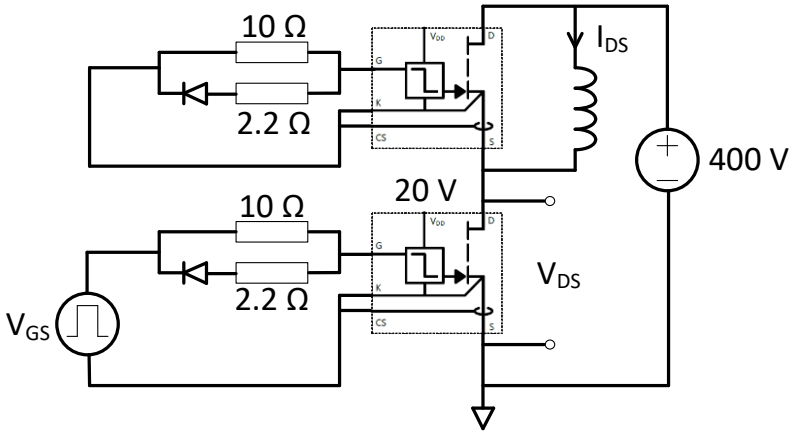
## Clamping power HEMT gate voltage

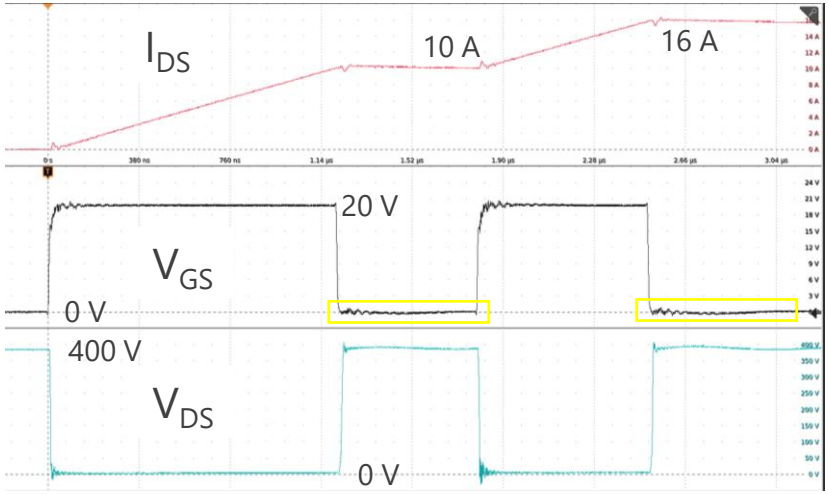


# EASE-TO-USE GAN HEMTS

## Miller clamp

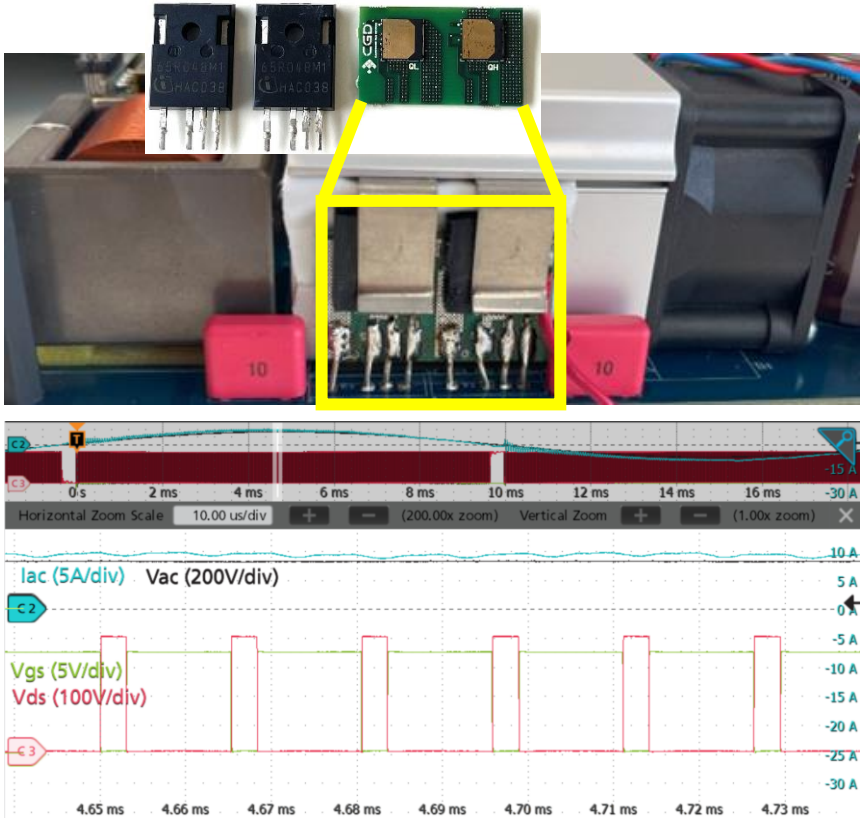
Double pulse test




Measured devices CGD65A055S2

Overcome return-on issue even had high parasitic inductance at source pin




ICeGaN 25 mohm top side cooled package.
Measured at 230 $V_{AC}$ input voltage and 10 $A_{(peak)}$ input current

# Measurement results
# 100 W 2C 1A PD

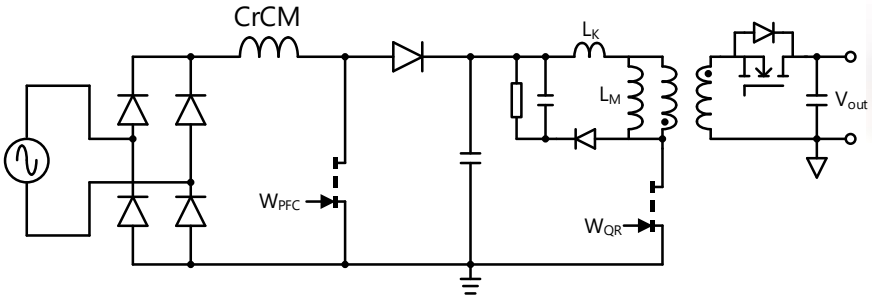
# 100 W PD REFERENCE DESIGN SPECIFICATION

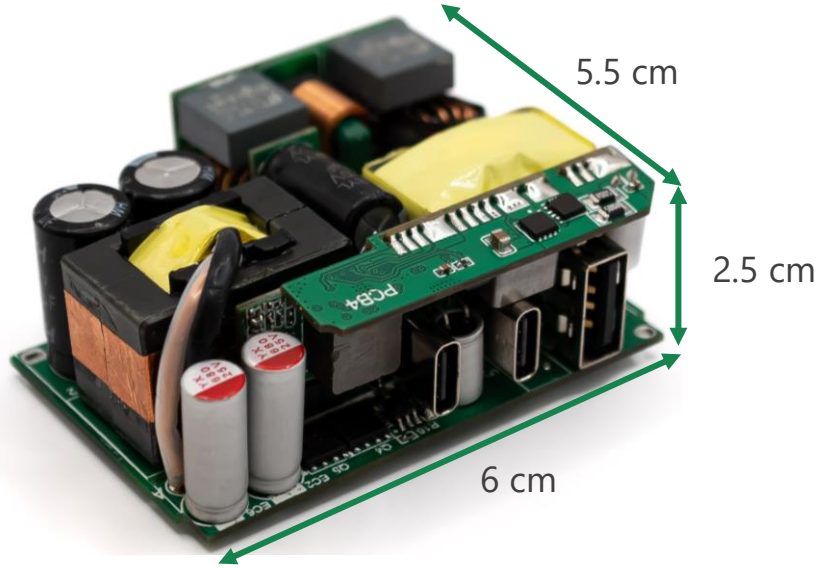
Input voltage: 90 Vac/60 Hz, 115 Vac/60 Hz, 230 Vac/50 Hz, 264 Vac/50 Hz

Output voltage: 5 V (3 A), 9 V (3 A), 12 V (3 A), 15 V (3 A), 20 V (5 A)

Power density (PCBA): 0.825 W/cm$^3$

CrCM boost + QR flyback + SR buck



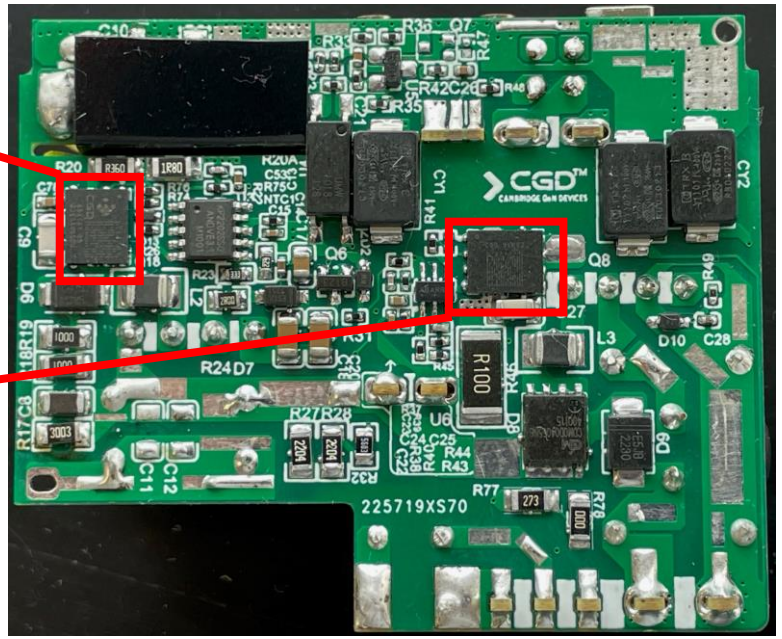



# TOPOLOGY AND DEVICE USAGE

CrM boost + QR flyback + SR buck

CrM boost ICeGaN:
CGD65B200S2
(200 mohm, 650 V,
DFN 5 x 6 )

QR flyback ICeGaN:
CGD65B240SH2
(240 mohm, 650 V, DFN 5 x 6 )
H2 series ICeGaN incorporates an advanced NL³ Circuit, leading to record low power losses at No Load and Light Load operations.



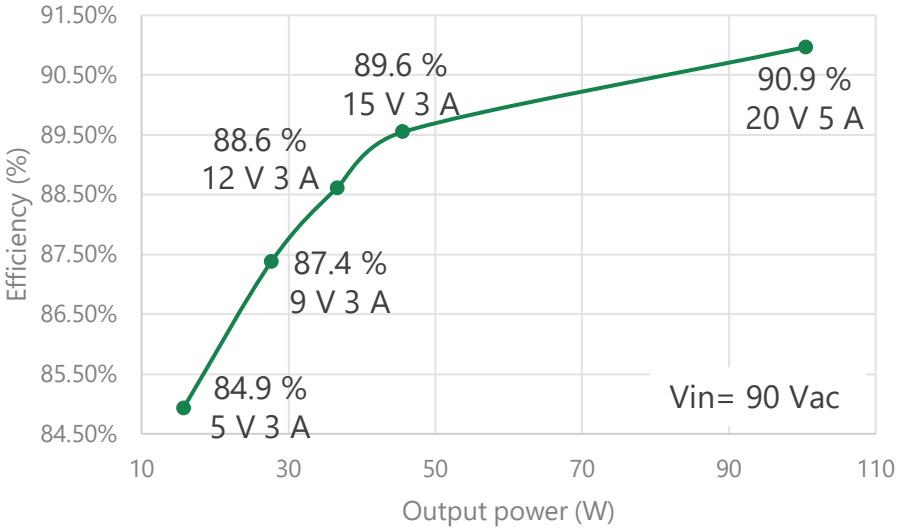
# NO LOAD POWER CONSUMPTION

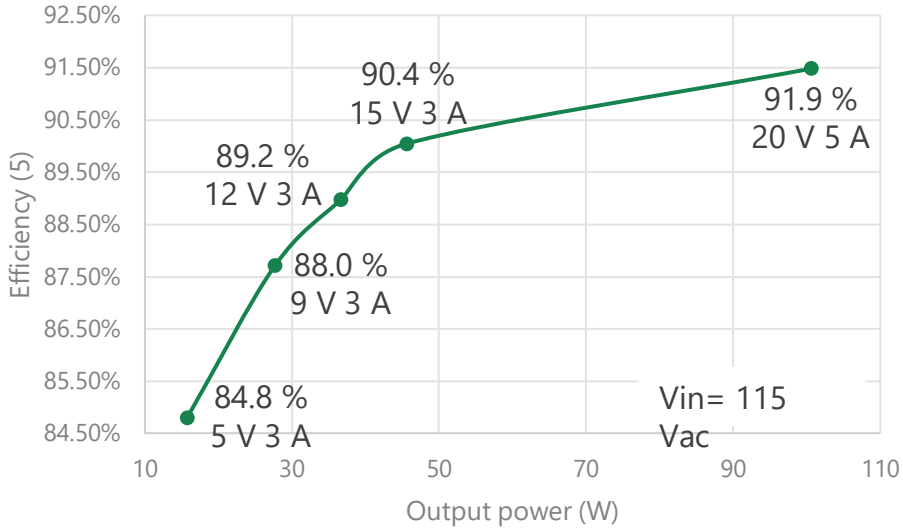
## Output voltage ports = 5 V

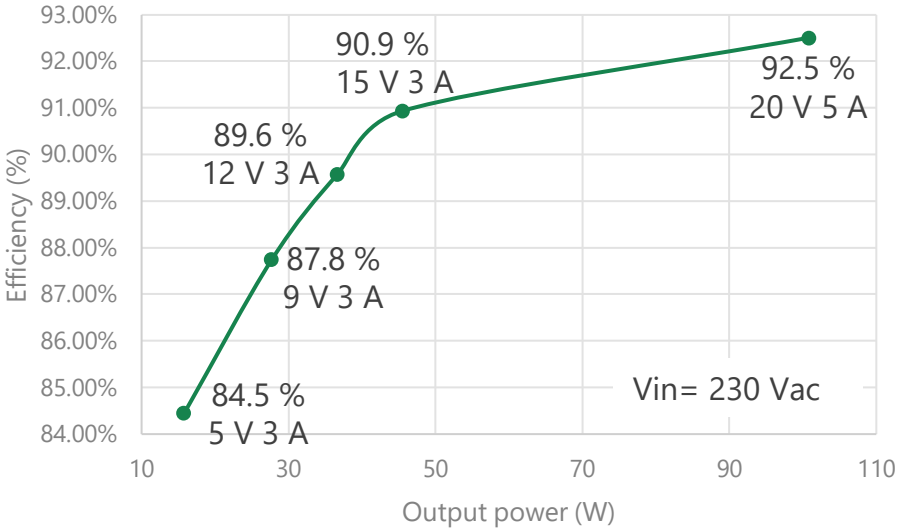
| Input voltage | No load input power only QR flyback | No load input power PFC stage + QR flyback | DoE Level VI 2016 | ErP 2020 |
|---|---|---|---|---|
| 90 V | 64 mW | 185 mW | ≤ 300 mW | ≤ 300 mW |
| 115 V | 74 mW | 195 mW | | |
| 230 V | 130 mW | 230 mW | | |
| 264 V | 150 mW | 284 mW | | |

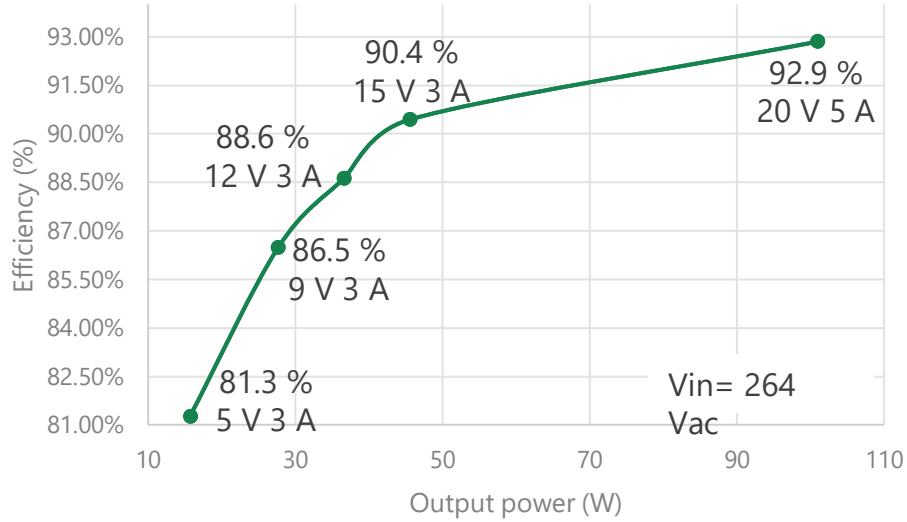
# EFFICIENCY MEASUREMENT AT TYPE C PORT

## Full load at different output voltage



# SUMMARY

The latest charger designs are requested low no-load power consumption, high efficiency, and high-power density

- no-low power consumption power reduce from 210 mW to 75 mW
- average efficiency increase from 88 % to 90.2 %

QR flyback is commonly selected topology in charger design

- minimize component count, easy control, low no load input power

GaN HEMT provides a linear and small output capacitor for fast discharging to achieve ZVS and reduces the switching losses at high switching frequency charger design

ICeGaN™ provides driving interface, $NL^3$ circuit, voltage limiter, and Miller clamp